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Knowledge to Wisdom

DIE TO DIE AND WITHIN DIE PROCESS VARIATION REDUCTION TECHNIQUE

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ABSTRACT

In this paper an analog adaptive body bias (A-ABB) circuit has been proposed. The A-ABB circuit is used to mitigate the impact of die-to-die (D2D) and within-die (WID) parameter variations. The main advantage of using this analog adaptive body bias technique is the circuit overhead. The A-ABB circuit provides lower overhead as compared to other biasing circuits. This circuit provides other advantages including circuit yield and also the speed, the dynamic power and the leakage power. The A-ABB circuit is derived using a sensing circuit to sense the value of the threshold voltage. This sensing circuit provides an approximation of the value of the voltage that is the varied due to die to die and within die process variation. After the sensing circuit a block of amplifier circuit is used in order to obtain the appropriate output value of the circuit. An analog control of the circuit is maintained through the amplifier circuit and maintains required body biasing voltage. In this circuit on-chip amplifier circuit is used. The simulation result of the following circuit can be calculated directly from the circuit or implementing the A-ABB circuit on some other basic circuit or even using Microprocessor

KEYWORDS*:* D2D, WID, A-ABB, Sensing Circuit, Circuit Yield, Dynamic Power

INTRODUCTION

Process variation has become an important parameter in almost all VLSI circuits. The change in the feature of the device due to limitation of the fabrication process is called process variation (e.g. L_{eff} = L ΔL). The process variation occurs due to the limitations of fabrication. The process variation has affected the performance in terms of frequency of the circuit. Process variation can be understood in terms of conformance, performance, features, reliability, durability and serviceability. The method involved in technical variation and economic results in worst process variation and intra-die device irregularities are elaborated in this chapter, especially with reference to yield of the product, reliability of the product and cost arising due to manufacture. Almost all of the semiconductor technology over the many decades is related directly or indirectly to the decreasing sizes of devices and circuits that allow increase in performance at a cost much lower. A similar consequence is that process variation increase with each technology point. Most of the analog circuits which are high performing rely on matched devices; this phenomenon has started to diminish yield of the device and reliability of chip fabrication. Probably, the problems that arise is that the parameters of circuits on the same die results in the increased intra-die variations, hence showing different characteristics. Also, we can see that V_{TH} shows dependence on length variation of the gate including the drain induced barrier lowering (DIBL) effect in condition of high drain source voltage bias. A direct effect of device parameter variations is reduction in yields because of block-level and system-level characteristics which show a corresponding higher level in variations. The direct relationship between variations and yield can be shown from the visualization in Figure 1.1, where the Gaussian distribution of a specification with a standard

deviation r around the mean value l is shown together with the specification limits (±3r in this example). For individual analog circuits, parameters such as gain may have an increased and/or decreased specification limit, and the products that exceed the limitation(s) while testing at the production phase must be discarded. Guard-bands are often defined as an account to measure uncertainties by being directed with the procedures by following the same test or switching towards more comprehensive tests to find whether the part can be sold to customers or not, which results in increased test cost while in a manufacturing environment. The complexities of system and process variations further raise the important part to consider testing early in the design phase so that any technical conditions and time-to market delays phase in the pre-production phase also test cost reduction during the production phase can be reduced. The most worst-case process corner circuits have been used in most cases to consider for variations at the time of design of analog circuits. In recent times, a shift at the use of statistical models and Monte Carlo simulations has raised.

TYPES OF PROCESS VARIATION

Parameter variations are further divided into following areas as spatial, temporal and NBTI.

Spatial Variations

The variation in the characteristics of the device when t = 0s is termed as spatial process variation. Such variations can be further divided into inter-die and intra-die process variations. Variations due to parameters among dies that come from altered runs, lots and chips are ranged into inter-die variations in comparison to variation of strengths of transistor within the same die which are termed as intra-die variations. Variations in length , width , flat-band conditions, thickness of the oxide etc., that will lead into inter-die process changes while line edge roughness (LER) or random do pant fluctuations (RDFs) will lead into intra-die random variations in case of process parameters.

Temporal Variations

Till now we have considered the impact of process variation on the characteristics of the device. Due to scaling of the dimensions, conditions on which the device operates of the ICs also change performance of the circuit.

NBTI

NBTI is the primary concern for reliability of Nano-scale transistors. In case of NBTI a continuous trap is generated in Si-SiO2 interface of p MOS transistors. NBTI is seen to be a threshold voltage shift in negative bias which has been applied to a MOS gate at elevated temperature, which mainly affects the p MOS transistors. In recent times, Negative-bias-temperature instability (NBTI) has become the main limiting factor of circuit life time. NBTI is considered as the generation of interface traps under negative bias conditions when $V_{gs} = -V_{dd}$) at elevated temperature in p MOS transistor. The threshold voltage device increases due to NBTI and when observed there is partial recovery, as soon as the stress is removed. In the bulk of MOSFETs, dangling Si bonds arises due to mismatch in the structure of the device at the Si-SiO2 interface which behaves as a charged interfacial traps. After oxidation when hydrogen passivation is applied at the silicon surface conversion of dangling Si atoms to Si-H atoms takes place. But with age and stress due to applied voltage the Si-H bonds break at the point of operation and again form the interfacial traps which henceforth increases Si atoms can be broken into Si-H bonds, which creates the interfacial traps and neutral H atoms. The H atoms which can either form H_2 molecules or can anneal any existing traps.

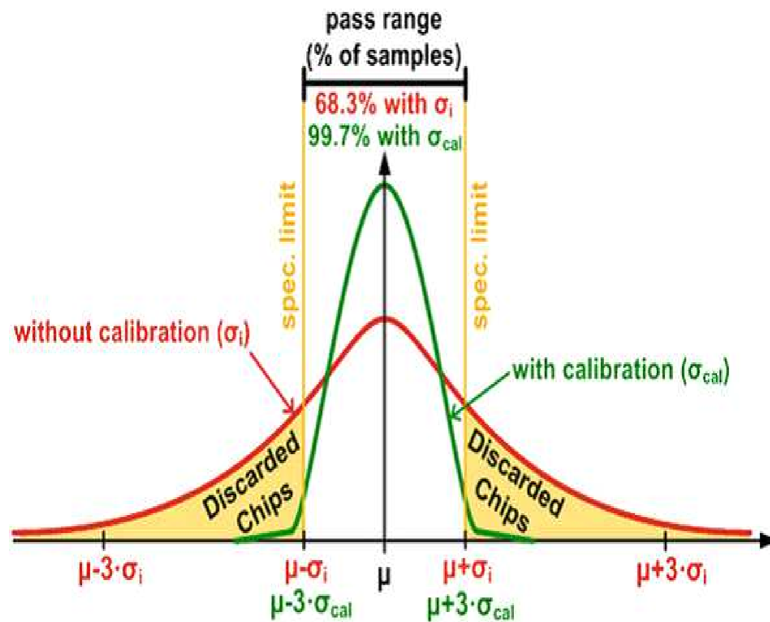

Figure 1: Consequences of Variation on Some Discarded Chip

DIE TO DIE AND WITHIN DIE PROCESS VARIATON

Process variations can also be classified as die-to-die (D2D) variations and within-die (WID) variations. In case of D2D variations, all the devices present on the same die are considered to have the same parameter values. However, when the devices on the same die are considered to behave differently, then they are said to be in WID variations. In most of the cases D2D variations are considered because it is one of the main factors of process variations, WID variations have become the most important design challenge as technology scales. The consumption of power is the one important challenge in today's high-performance designs and circuits. Significantly, the other factor that places a design challenge is to maintain the variability in device and circuit parameters. The scaling in process technology the affect of variations on the circuit parameters becomes more pronounced especially in the range of 65nm and beyond, the effect of variations on the maximum clock frequency (FMAX) and power of a circuit is expected to get worst. The integrated circuit (IC) fabrication technique in the sub-100nm regime is complicated but accurate. One of the major concerns of process variation is WID variation. As it deviates the performance of integrated circuits from their original intent. The deviations hence caused reduce the yield and revenues from integrated circuit fabrication. A D2D variation, resulting from lot-to-lot, wafer-to-wafer, and a portion of the within-wafer variations, has been affecting the characteristics of all transistors and interconnects of a die equally. Henceforth, different electrical characteristics within a die results into WID variations which consist of random and systematic components which will be induced. A random-WID parameter variation varies randomly and unconventionally from device to device (i.e., device-to-device interaction is zero). A systematic-WID parameter variation that results from a quotable and governing principle, where the device-to-device correlation is determined empirically as a function of the distance between the devices. A correlated behaviour is exhibited by systematic WID variations. From die to die the profile of these variations can randomly change. As a designer's perspective is concerned, systematic-WID variations behave as sustained and smooth correlated random WID variations. Various core processors are rising as a power-efficient approach to fabricate high-performance microprocessors. In variation to large single-core processors, many multi-core processors exhert a number of less complex cores on a die, in which the number of cores and core complexity is the most important design trade-off. Multi-core processors will achieve much better performance on

highly parallel multithreaded applications which execute the threads across the cores parallel to operating at a lower clock frequency and lower power. When designing high-performance microprocessors, the major effect of accurately estimating the effect of parameter variations on product-level performance which directly relates to the overall revenue of a company. Whenever a circuit is overestimated for rise in design complexity it leads to an increase in design time, an increase in size of the die. The design with good manufacturing is rejected due to a small yet complex issue of variability and even missed market windows. Reversely, an underestimation will compromise product performance and overall yields. In summary, overestimating variations will impact the design effort, and underestimating variations will effect the manufacturing effort.

Impact of PV and NBTI on Devices

Process parameters variation and NBTI affect device characteristics which limit to continue scaling of transistor dimensions. Process variation and NBTI increases threshold voltage. Threshold voltage variation results not only in limited supply voltage scaling but also it affect the accuracy of estimation of leakage power. Different circuits suffer from different process variation. The process variation in p-MOS transistor circuits is affected by static NBTI during active mode and age very simultaneously, so the aging has to be explicitly addressed. Circuits which are designed without taking into account process variations and NBTI, usually fails to meet the desired timing, power, stability, and quality specifications.

DIE TO DIE AND WITHIN DIE MITIGATION TECHNIQUE

In this paper an analog adaptive body bias (A-ABB) circuit has been proposed. The A-ABB circuit is used to mitigate the impact of die-to-die (D2D) and within-die (WID) parameter variations. The main advantage of using this analog adaptive body bias technique is the circuit overhead. The A-ABB circuit provides lower overhead as compared to other biasing circuits. This circuit provides other advantages including circuit yield and also the speed, the dynamic power and the leakage power. The A-ABB circuit is derived using a sensing circuit to sense the value of the threshold voltage. This sensing circuit provides an approximation of the value of the voltage that is the varied due to die to die and within die process variation. After the sensing circuit a block of amplifier circuit is used in order to obtain the appropriate output value of the circuit. An analog control of the circuit is maintained through the amplifier circuit and maintains required body biasing voltage. In this circuit on-chip amplifier circuit is used. The simulation result of the following circuit can be calculated directly from the circuit or implementing the A-ABB circuit on some other basic circuit or even using microprocessor. Circuit level simulation of a block is extracted from a microprocessor circuit. The study of A-ABB circuit at industrial hardware level shows that the proposed circuit reduces the standard deviations of the frequency, the dynamic power and the leakage power. The advantage of the proposed circuit is its lower area overhead allowing it to be used at lower granularity level than that of the previously published circuits

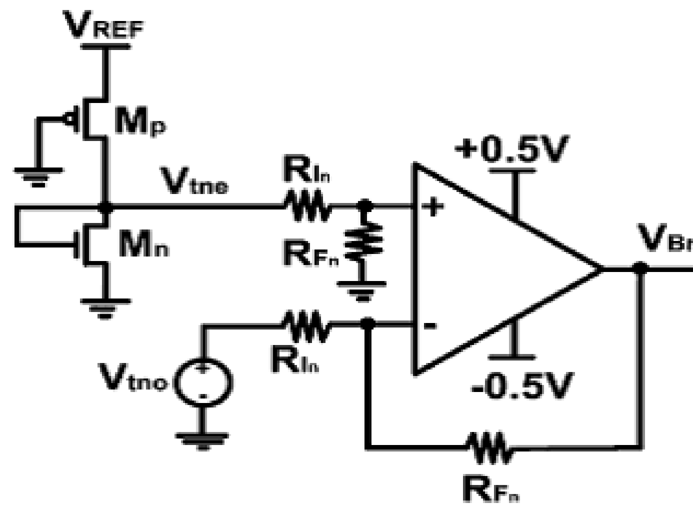

Figure 2: Proposed Circuit A-ABB for n MOS

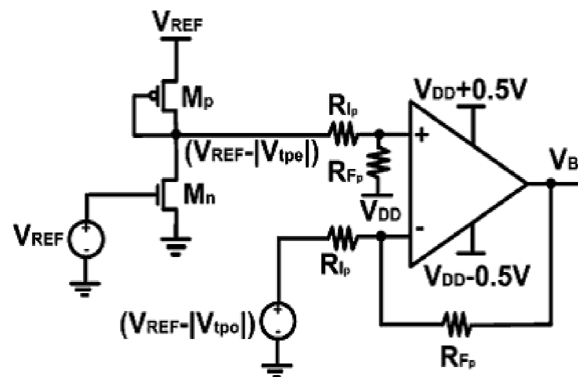

Figure 3: Proposed Circuit A-ABB for p MOS

The circuit is impacted by die to die and within die process variation due to which the value of the threshold voltage of the circuit is either increased or decreased and the original value of the circuit does not remain same. In A-ABB circuit the increased or decreased value of the threshold voltage V_T is sensed by the sensing circuit and it is compensated by stabilizing and maintaining the value of the original circuit. The critical path of the circuit is set in order to keep the estimation circuit i.e., the sensing circuit close to the value of the original circuit. The next block in the A-ABB circuit is the controlling amplifier circuit which control the body bias voltage of the circuit.

The A-ABB circuit provides a related area overhead and an associated granularity level of the circuit. The granularity level of the circuit is directly proportional to the area overhead i.e., the lower the granularity level the higher the area overhead. The other ABB circuits are not efficient for random WID variation as a mitigation technique. The high performing logic circuits mostly digital circuits are strongly affected by spatially inter-related channel length variation which can be compensated using this technique.

SIMULATION WORK

In order to increase the density of the chip with the size of the transistor has to be scaled down which results into process variation. Leading to the problem of process variation is leakage power. Leakage power accounts for an increasingly larger value of sum total of power consumption in deep submicron technologies. The method of active leakage

reduces leakage power by randomly disconnecting supply to inactive blocks and hence adjusting body bias to more limit leakage and further improving performance. The control scheme of active leakage is important for blocks with decreasing activity factors and relatively long idle periods. A very large proportion of functional blocks which are digital in nature are only active for a tiny fraction of time. When the functional block is not in the state of operation, leakage still occurs. In technologies such as deep sub-micron, phenomenon of this type is aggravated due to the reduction in threshold voltage due to scaling. Leakage power in this circuit is up to about 40.5% of total value of power consumption in today's high performance microprocessors. Leakage power reduction has always become the key to a very low power design. There is an increase in optimum reverse body bias, which is unique to any technology generation, that reduces the standby leakage power consumption of an IC design implemented in that technology. V, scaling causes the sub-threshold leakage current of the transistor to increase exponentially, which results in unacceptably large standby power consumption in mobile designs. Process parameter variations, which are becoming worse as technology scales, impact the frequency and leakage distribution of fabricated microprocessor dies. Due to these die-to-die and within-die variations, some dies cannot achieve the desired frequency target, while many others do not reach the maximum leakage power specification. In the same way, some circuits with high leakage power may fail when subjected to the burn-in reliability test at elevated supply voltage and temperature. Bi-directional adaptive body bias (VBS) has been employed to reduce the impact of these variations and increase the number of high-frequency processors. The body-to source bias voltage is increased considerably and therefore in this scheme the threshold voltage (VT) of the NMOS and/or PMOS transistors within the die is maintained at constant level. Each die receives a unique body bias – either forward (FBB), zero, or reverse (RBB) – which maximizes the die frequency subject to the leakage constraint. Dies which are too slow receive forward body bias to increase the frequency while dies which fail the maximum leakage specification are reverse-biased. The frequency of the circuit and leakage of the processor within a die can be controlled through adaptive change of the supply voltage (VCC). We consider here both the switching and leakage components of power consumption which have a super-linear relation to VCC, changing the supply voltage has a significant impact on the total power consumption. The effectiveness of adaptive supply voltage and frequency binning, used individually and in conjunction with adaptive VBS, for improving distributions of die frequency and power in low power and high performance microprocessors. We compare usefulness of these schemes for maximizing the percentage of dies accepted in the highest frequency bins, subject to constraints of total active power, burn-in leakage power and standby leakage power. Most of the integrated circuits have always been easily affected and harmed due to essentially die-to-die and within-die fluctuations in the process of manufacturing. Traditionally, die-to-die fluctuations have been the main problem for CMOS digital circuits. In order to control the value of die-to-die fluctuation the circuit is generated but within-die fluctuations is more or less neglected. The poly-silicon gate lengths have reduced below a certain level of the wavelength of light used in the optical lithography process, but much importantly, the systematic and random within-die variations of channel length have increased within the die-to-die fluctuations. With the scaling of the MOSFET's, the variation in the location of doping atoms of the device active region induces drain current fluctuations. Such an effect is intrinsic which cannot be eliminated by the control of external conventional processes of manufacturing. Thus, within-die to die fluctuations is a growing menace to the performance and functionality of future Giga scale integration (GSI) circuits. POWER density has become a significant concern in microprocessor design due to a huge size of transistors which are integrated on a single die with the increase in clock frequencies. The density of power which leads to limitation of a processor is dictated by the thermal design of the system, hence impacts system cost and highest operating frequency. The constraints of power are even more stringent in processor designs most importantly in mobile in

which high battery life is desirable. Also at the same time, processors must achieve high frequencies under this power constraint. The main objective of most the processor design is to limit the leakage in power consumption and therefore to achieve this goal the maximum operating frequency is maintained while meeting the power density constraint. Process parameter variations have always resulted in fabrication of dies with variations in highest operating frequency and consumption of power. Within-die to die variations results into differences in characteristics of transistor through a single die. The value of device parameters within the same die changes most of the time with change in the single die parameters. To summarize further, these variations result in a dispensation of frequencies of die and leakages. Usually the distribution of parameter values is done in such a manner so that the overall value of the circuit remains constant with change in the value of external factors. The several regions or "bins" are categorized according to the value of the device parameters and the change in these parameters. The microprocessors are kept into the maximum possible frequency bin which meets the power specification. Most of the dies are not accepted either due to minimum operating frequency or very high power consumption. The significance of correctly estimating the outcome of parameter variations on circuit performance is specifically related to a company's overall revenue. An overestimation of the die size ultimately increases the design complication which possibly leads to a rise in design time, an increase in die size, rejection of otherwise good designs and even missed market windows. Reversely, an underestimation will only compromise the product's performance and overall yield as well as increase in the silicon debugs time. In summary, overestimating fluctuations affect the design effort, and underestimating variation which impacts the production and manufacturing effort. A very successful design of digital integrated circuits has mostly relied on complicated optimization within various design specifications which includes silicon area, speed, testability, design effort and power dissipation. This traditional design approach mostly assumes that the electrical and physical properties of transistors are predictable and also deterministic over the device lifetime. Nevertheless, with the silicon technology which enters the sub-100nm regime, transistors will no longer act deterministically over time. The significant phenomenon that causes such a change is the temporal reliability in MOSFETs due to the Negative Bias Temperature Instability (NBTI). Much work has been done to eliminate the effect of process variation at various level of abstraction (device / circuit /architecture). A lot of techniques have been proposed to compensate for the effect of process and NBTI effect but even these techniques have drawbacks. Techniques we are talking about are mostly related here to body biasing techniques. Adaptive body bias (ABB) is a technique which allows the variation in the threshold voltage of the transistor by maintaining the value of the transistor body-to-source voltage. A compensating circuit like a forward body bias (FBB) (i.e., $V_{SB}>0$) decreases the voltage Vt which is the threshold voltage of the circuit, consequently rising the device speed at the cost of increased leakage power. Similarly, a reverse body bias (RBB) (i.e., $V_{SB}<0$) increases, which decreases the leakage power but with the disadvantage of slowing the device. The seriousness of NBTI degradation at the device level requires immediate research of the problem at the circuit level. Nevertheless, if dependent on the particular topology and working condition, degradations at the level of circuit considering NBTI can show a huge variation. In the present technique, two important application of the circuit have been considered which are random logic and memory arrays and then have compared the various NBTI induced performance. We further determine the seriousness of NBTI based on the qualitative analysis of such circuits, and then efficient reliability-aware design techniques can be proposed to likely reduce or minimize the effect of NBTI. In comparison to the existing technique, the one proposed here takes into consideration the required benefits of a biasing circuit and eliminates its disadvantages. Such techniques that are sensitive to change and are reliably aware in terms of the actual design effort and complexity. The study will provide an extensive explanation of NBTI degradation in circuits, and it will attract a

universal design procedure for logic and memory design for NBTI-tolerant. Two way directional adaptive body bias (ABB) are mostly utilized to mitigate for die-to-die parameter variations. By applying best p MOS and n MOS body bias voltage in each die which increases the die frequency which results to a power constraint. If we further elaborate such a technique that mitigates for within-die to die parameter variations as well hence increases the number of dies accepted in the highest frequency bin. ABB is therefore found to maintain improvement in the presence of increasing process parameter variations.

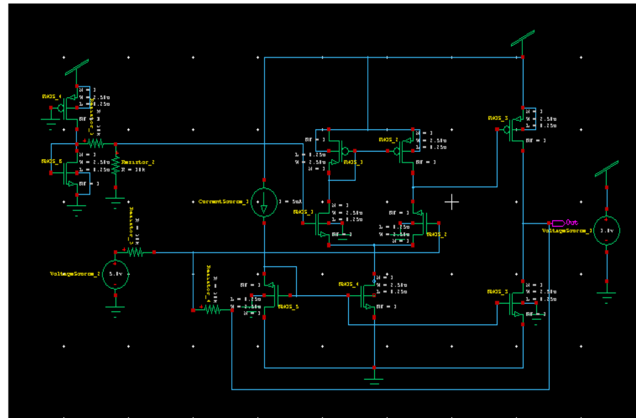

Figure 4: A-ABB Circuit

Below are the waveforms from the simulation .Here it gives the correct result and output nodes are correctly exited as per the input.

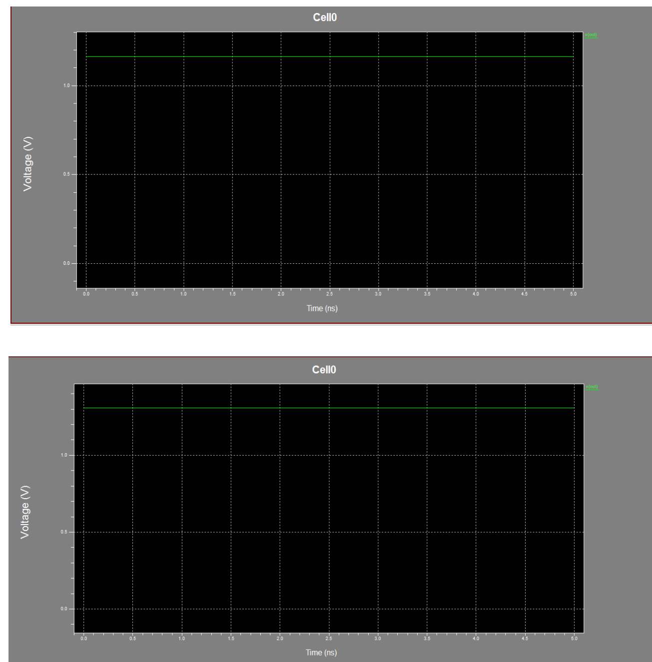

Figure 5: Simulation Result of A-ABB Circuit at 1V and 3V of Threshold Voltage of Sensor Circuit Vtp

CONCLUSIONS

From The continuance in technology scaling defines a benchmark on the scaling of voltage that is provided. So in order to make absorption of power minimal with the latest structure is the requirement of design in modern integral circuitries. In view of today's going need of scaling the leakage power can be further reduced in the range of nanometers.

Also the requirement of power can be further reduced with the growing technology. Improvement in circuit of Analog Adaptive Body Bias extension of schema for operation, it peruses a lead to immense reduction in die to die and within die process variations.

Table 1: Different Input and Output Plot

S.NO	V_{tp} of Sensor Circuit(V)	V_{BN} of Proposed Circuit(mV)
1.	1	1.3
2.	2	1.0
3.	3	1.15
4.	4	1.21
5.	5	1.3

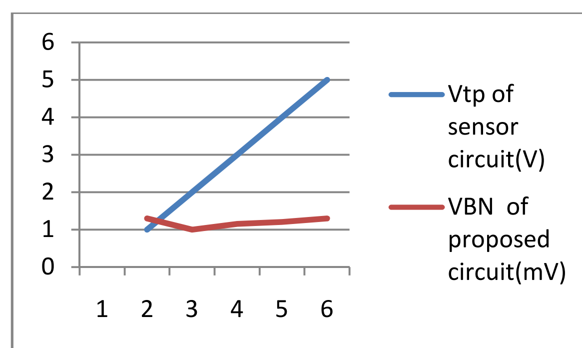

Figure 6

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